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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,450	12/02/2004	Chen-Chih Huang	SUND 501CIP	3611
23995	7590	09/14/2006	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005				NGUYEN, LINH M
		ART UNIT		PAPER NUMBER
		2816		

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/773,450	HUANG ET AL.
	Examiner Linh M. Nguyen	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12/02/04 & 10/25/05.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-16 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 09 February 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 10/079,866.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Claim Objections/Minor Informalities

1. Claims 1 and 9 are objected to because of the following informalities:

Claims 1 and 9, line 9 (starting with “signal is”), change “fist” to --first--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4-9 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant’s Admitted Prior Art (Fig. 1A) in view of Tomobe et al. (U.S. Patent No. 6,198,334).

With respect to claims 1, 4-7, 9 and 12-15, the Applicant’s Admitted Prior Art (Fig. 1A) discloses a phase-interpolation circuit for outputting a third clock signal, the circuit comprising (1) a first inverter [11] for receiving a first clock signal [CK1], and (2) a second inverter [12] for receiving a second clock signal [CK2], and an output end connected to an output end of the first inverter to form a common output end [V0] to output the third clock signal; in which the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal.

The Applicant’s Admitted Prior Art (Fig. 1) does not disclose a detailed configuration of the inverters, including (1) a first controlled switch connecting between the first inverter, the

second inverter, and a power source; wherein the first controlled switch is (i) “OFF” when the first clock signal is in a first state (*or when both the first and second double-level clock signals are in the first state*), and (ii) is “ON” when the first clock signal is in a second state (*or when both the first and second clock signals are in the second state*), (2) a second controlled switch connecting between the first inverter, the second inverter, and ground; in which (i) the second controlled switch is “ON” when the first clock signal is in the first state (*or when both the first and second clock signals are in the first state*), and (ii) is “OFF” when the first clock signal is in the second state (*or when both the first and second clock signals are in the second state*), (3) (including limitations claimed in claim 4) a first PMOS connecting between the first inverter and the power source, being “OFF” when the first clock signal is in the first state, and being “ON” when the first clock signal is in the second state; a second PMOS connecting between the second inverter and the power source, being “OFF” when the second clock signal is in the first state (*or when both the first and second clock signals are in first state*), and being “ON” when the second clock signal is in the second state (*or when both the first and second clock signals are in second state*), and the first controlled switch and the second controlled switch are to avoid a short circuit current of the phase-interpolation circuit (4) (including limitations claimed in claim 5) a first NMOS connecting between the first inverter and the ground, being “OFF” when the first clock signal is in the second state (*or when both the first and second clock signals are in the second state*), and being “ON” when the first clock signal is in the first state (*or when both the first and second clock signals are in the first state*); a second NMOS connecting between the second inverter and the ground, being “OFF” when the second clock signal is in the second state (*or when both the first and second clock signals are in the second state*), and being “ON” when the

first clock signal is in the first state (*or when both the first and second clock signals are in the first state*), (5) (including limitations claimed in claim 6) the first controlled switch being (i) a PMOS, and (6) (including limitations claimed in claim 7) the second controlled switch being (i) an NMOS.

Tomobe et al. discloses, in Figs. 1 and 5, a detailed configuration of a CMOS inverter circuit (in figure 1) and a truth table for the CMOS inverter circuit operation (in figure 5). The CMOS inverter circuit of Tomobe et al. in figure 1 comprises (1) an input end [INPUT TERMINAL], (2) a first controlled switch [P1], (3) a CMOS inverter [P2, N2], and (4) a second controlled switch [N1]; wherein all [P1, P2, N1, N2] are connected in series.

To modify the phase interpolation circuit of the Applicant's Admitted Prior Art (Fig. 1A) by configuring in the CMOS inverters of the Applicant's Admitted Prior Art (Fig. 1A) with the PMOS and NMOS transistors connected in series in each inverter to cause switching speeds of the transistors and thus to improve the noise resistance performance of the phase interpolation circuit would have been obvious to one of ordinary skills in the art at the time of the invention since such a configuration of the PMOS and NMOS transistors in the CMOS inverters for the stated purpose has been a well-known practice in the art as evidenced by the teachings of Tomote et al. (see Tomobe et al.; Abstract, lines 1-7).

With respect to claims 8 and 16, the Applicant's Admitted Prior Art (Fig. 1A) teaches that the inverters are CMOS inverters (see page 4, line 6, of the specification of the instant application).

4. Claims 2-3 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1A) in view of Tomobe et al. (U.S. Patent No. 6,198,334) as applied to claims 1 and 9 above, and further in view of Kim (U.S. Patent No. 6,225,847).

With respect to claims 2 and 10, the combined teachings of the Applicant's Admitted Prior Art (Fig. 1A) and Tomobe et al. disclose all of the claimed limitations as expressly recited in claims 1 and 9 above, except for a third inverter having (i) an input end connected to the common output end, and (ii) an output end for outputting a third clock signal.

Kim discloses, in Fig. 2, a CMOS clock generating circuit comprising an inverter [INV3] which has (i) an input end [34] connected to the common output end [output of element 3], and (ii) an output end for outputting a clock signal [Clk].

It would have been obvious to one of ordinary skill in the art at the time of the invention to additionally configure in the interpolation circuit of the combination The Applicant's admitted Prior art (Fig. 1A) and Tomobe et al. an inverter having an input end for connecting to the common output end (of the phase interpolation circuit of the combination) and an output end for outputting a clock signal as taught by Kim to obtain an inverted and buffered output clock signal since such an arrangement of the additional inverter would provide a complementary output clock signal that would be needed for a specific application to acquire an optimal performance.

With respect to claims 3 and 11, the combined teachings of the Applicant's Admitted Prior Art (Fig. 1A) and Tomobe et al. disclose all of the claimed limitations as expressly recited in claims 1 and 9 above, except for (1) an inverter (or a fourth inverter as claimed) having an output end connected to the first inverter in order to output the first double-level clock signal to the input end of the first inverter, and (2) another inverter (or a fifth inverter as claimed) having

an output end connected to the second inverter in order to output the second double-level clock signal to the input end of the second inverter.

Kim discloses, in figure 3, the configuration of an inverter [11] having (i) an input end [N1] connected to an input clock signal [Clk], and (ii) an output end [N2] for outputting an inverted clock signal [Clk\] to an input end [22] of an inverter [QP11, QN12]. Kim does not teach another inverter for a respective second inverter.

However, this practice of configuring an inverter for receiving an input clock signal and outputting an inverted clock signal to another inverter would provide complementary clock signals of exact phase and timing (see Kim, col. 2, lines 39-49), that would be needed for a specific application to acquire an optimal performance. For such an advantage, to implement the phase interpolation circuit of the combination The Applicant's Admitted Prior Art (Fig. 1A) and Tomobe et al. by arranging an inverter for receiving the input clock signal and outputting an inverted clock signal to a following inverter as taught by Kim would have been deemed obvious to a person skilled in the art.

Citation of Relevant Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Tomisawa (U.S. Patent No. 5,012,141) discloses a signal delay device using CMOS supply voltage control.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is 571-272-1749. The examiner can normally be reached on 7-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LMN



LINH M. NGUYEN
PRIMARY EXAMINER